



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Attorney Docket No.: LOVO-041.DIV

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Date of Deposit:	01/19/04	Name of Person Making the Deposit:	Shannon Carmo	Signature of the Person Making the Deposit:	Shannon Carmo
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Inventor(s): Pete L. Pegler

Serial No.: 10/677,570

Group Art Unit:

Filed: 10/01/2003

Examiner:

Title: METHOD FOR A JUNCTION FIELD EFFECT TRANSISTOR WITH REDUCED GATE CAPACITANCE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CORRECTED FILING RECEIPT

1. Attached is a copy of the official filing receipt received from the PTO in the above application for which issuance of a corrected filing receipt is respectfully requested.
2. There is an error with respect to the following data, which is:
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and/or
 omitted.

Error In

Correct Data

- | | |
|----------------------------|---|
| 1. [] Applicant's name | 1. |
| 2. [] Applicant's address | 2. |
| 3. [] Title | 3. |
| 4. [] Filing Date | 4. |
| 5. [] Serial Number | 5. |
| 6. [] Foreign/PCT | 6. |
| 7. [X] Other | 7. (Domestic Priority data as claimed by applicant) 10/278,303 10/22/02 |

3.

- A. The correction(s) is/are not due to any error by the Applicant and therefore no fee is due.

OR

- B. At least one of the above corrections is due to applicant's error and the fee therefore, under CFR 1.19(h), of \$25.00 is paid as follows:

Enclosed is check for \$25.00.

Charge Account 23-0085 \$25.00.

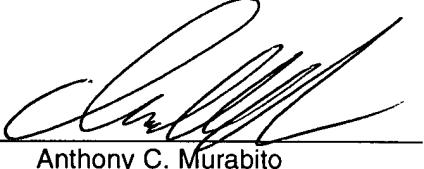
Please direct all correspondence concerning the above-identified application to the following address:

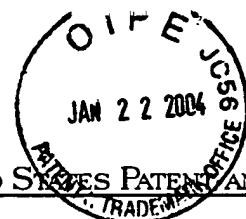
WAGNER, MURABITO & HAO LLP
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Respectfully submitted,

Date: 1/19/2004

By:


Anthony C. Murabito
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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/677,570	10/01/2003	2811	856	LOVO-041.DIV	7	20	4

WAGNER, MURABITO & HAO LLP
 Third Floor
 Two North Market Street
 San Jose, CA 95113

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FILING RECEIPT



OC000000011568927

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Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

Pete L. Pegler, Mesa, AZ;

Assignment For Published Patent Application

Loveltech, Inc.;

Domestic Priority data as claimed by applicant

This application is a DIV of 10/287,303 11/03/2002 *

(*)Data provided by applicant is not consistent with PTO records.

Foreign Applications**If Required, Foreign Filing License Granted:** 12/24/2003**Projected Publication Date:** Request for Non-Publication Acknowledged**Non-Publication Request:** Yes**Early Publication Request:** No**Title**

Method for a junction field effect transistor with reduced gate capacitance

DOCKETED
 Date: 1-19-04
 Initials: CDB

Preliminary Class

257

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